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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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1. INVENTOR(S)

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2. TITLE OF THE INVENTION

DFT TECHNIQUE FOR STRESSING THE SELF-TIME SEMICONDUCTOR MEMORIES TO DETECT DELAY FAULTS

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PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

4. ENCLOSED APPLICATION PARTS

☒ Specification **(11 pages)**
☒ Drawing(s) **(4 sheet(s))**
☒ Return-Receipt Postcard

5. METHOD OF PAYMENT

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number **14-1270.** Filing Fee Amount: **$160**

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Respectfully submitted,

By Peter Zawilski

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DFT Technique for Stressing the Self-timed Semiconductor Memories to detect delay faults

Mohamed Azimane and Ananta Majhi
22 September 2003

Abstract

The invention introduces an efficient solution to increase the controllability to catch dynamic defects which cause delay faults and which may escape the test even when the correct test patterns are applied. The correct test patterns may result to low fault coverage when the correct stress conditions are not satisfied. The fault coverage is increased when the correct test patterns are combined with the correct stress conditions. It has been shown that a duty cycle other than 50% at the internal clock of the address decoder helps to detect the resistive open defects that lead to slow-to-rise and the slow-to-fall delays. However, nowadays the semiconductor memories are self-timed, and the corresponding actions for initiating and controlling the read and write operations are independent of the external clock. The read and write cycles in the self-timed memories are both triggered by either the positive or the negative edge of the clock. Thus, any deviation of the clock duty cycle from 50% does not disturb the function of the memory. This invention introduces a simple DFT technique to stress even more the sensitising operation by controlling internally the beginning and the end of read/write operations.

1. Problem statement

Self-timed memories are well known in the art and are used in high-speed SOCs [1]. The read and write cycles in the self-timed memories are triggered by either the rising or falling edge of the clock, the memory cycle continues until the completion independent of the falling or rising clock edge, respectively. It has been already shown in an earlier patent [2] that a duty cycle different than 50% has different effect on the delay fault coverage. A smaller duty cycle than 50% helps to detect the resistive open and bridge defects that cause slow-to-rise behaviour in the memory address decoder. A higher duty cycle than 50% helps to detect the resistive open and bridge defects that cause the slow-to-fall behaviour in the memory address decoder. In fact, the duty cycle of the clock may stress also the sense amplifiers, the bit lines, the precharge and the discharge circuitry. This also increases the delay fault coverage of the memories. Moreover, it is already known that at-speed testing stresses the delay faults when the correct test patterns are implemented [2]. However, the synthesis of the BIST logic for high frequency is not always feasible and may lead to an extra area overhead. Therefore, finding a better solution than at-speed testing helps in increasing the fault coverage of the semiconductor memories.

Patent [2] shows the fault coverage dependency on the duty cycle. For specific duty cycles (other than 50%), the fault coverage of the delay faults is increased. However, changing the duty cycle of the clock has no effect on the fault coverage for self-timed memories, because the falling or the rising edge of the clock cannot control the end of the clock cycle. The memory decides internally when the read/write operation must be terminated depending on the dummy blocks. Thus, the

controllability of the sensitising operation remains unfeasible by increasing or reducing the duty cycle of the clock.

Moreover, the resistive open defects are becoming the dominant defects due to the change from Aluminum backend to Cupper backend. In Aluminum backend (up to CMOS 18), the resistive bridges are more dominant than resistive opens. In Copper backend (CMOS 12 and beyond), resistive opens are more dominant than ever before. Therefore, the upcoming technologies will highly suffer from the resistive open defects. Thus, we have to improve the test quality targeting the delay faults for better quality products, reduced reliability risks and customer returns (PPM).

2. Disadvantages

In the self-timed memories, the duty cycle effect disappears in a normal functioning of the memory due to the self-timed operations. The memory itself decides when the read/write operation has to be finished. Controlling the beginning or the end of an action in an internal memory block becomes impossible because of the self-timing used in nowadays memories. Thus, the controllability of the internal memory blocks is lost. Therefore, the correct test patterns to cover resistive open defect and resistive bridge defects that may lead to delay faults must be applied at-speed. Otherwise, the test patterns will not add any value to the fault coverage. Making a BIST that runs at the same memory frequency may be costly in terms of extra area overhead. On the other hand, the uncontrollability of the beginning and the end of an internal operation in specified memory blocks is making memory test a difficult task for detecting slow-to-rise and slow-to-fall delays. This will lead to fault coverage loss, reduce the product quality, increase the reliability risks and increase the customer returns (PPM).

3. Proposed solution

We propose a new and efficient solution to increase the controllability of the internal block of the memory in such a way, that the duty cycle becomes a parameter which impacts the fault coverage of the delay faults. With this solution we will be able to control internally the beginning and the end of determined internal operations in the memory by introducing a simple DFT technique. Therefore, modifying the duty cycle of the clock can easily control the internal memory blocks that have a big impact on the memory fault coverage. For instance, the row address decoder is a block that can be controlled to cover small delay faults at the word lines due to weak resistive open defects. Figure 1 shows a 2 to 4 address decoder controlled by an internal clock PHIX. The control logic (i.e., the clock monitor) is initiated based on the rising or the falling edge of the external clock CL and it generates an internal clock PHIX. This controls the word line activation and deactivation depending on the rising or the falling edge of the internal clock. Hence, the deactivation of the word lines becomes independent of the external clock CL. As we have shown in patent [2], the impact of the duty cycle on the detection of the slow-to-rise and the slow-to-fall depends extensively on the waveform of the internal clock. The slow-to-rise and the slow-to-fall delay faults can only be detected by controlling the duty cycle of the internal clock and not the external clock. The internal clock of the address decoder can be easily controlled by introducing a simple MUX in between the internal clock and the external clock. In this way, the external clock will be directly applied to the

address decoder during test mode. In normal mode, the self-timed control will be operating. Thus, the beginning and the end of the activation and deactivation of the word lines will be easily controlled from the external clock. Figure 2 shows a 2 to 4 address decoder with a MUX in between the address decoder clock input and the external clock. This technique can also be extended to cover all internal memory blocks that controlled by the internal memory clock, those are: the sense amplifier, the column and the bank decoder, the precharge and the discharge circuitry, and finally the input/output latches.

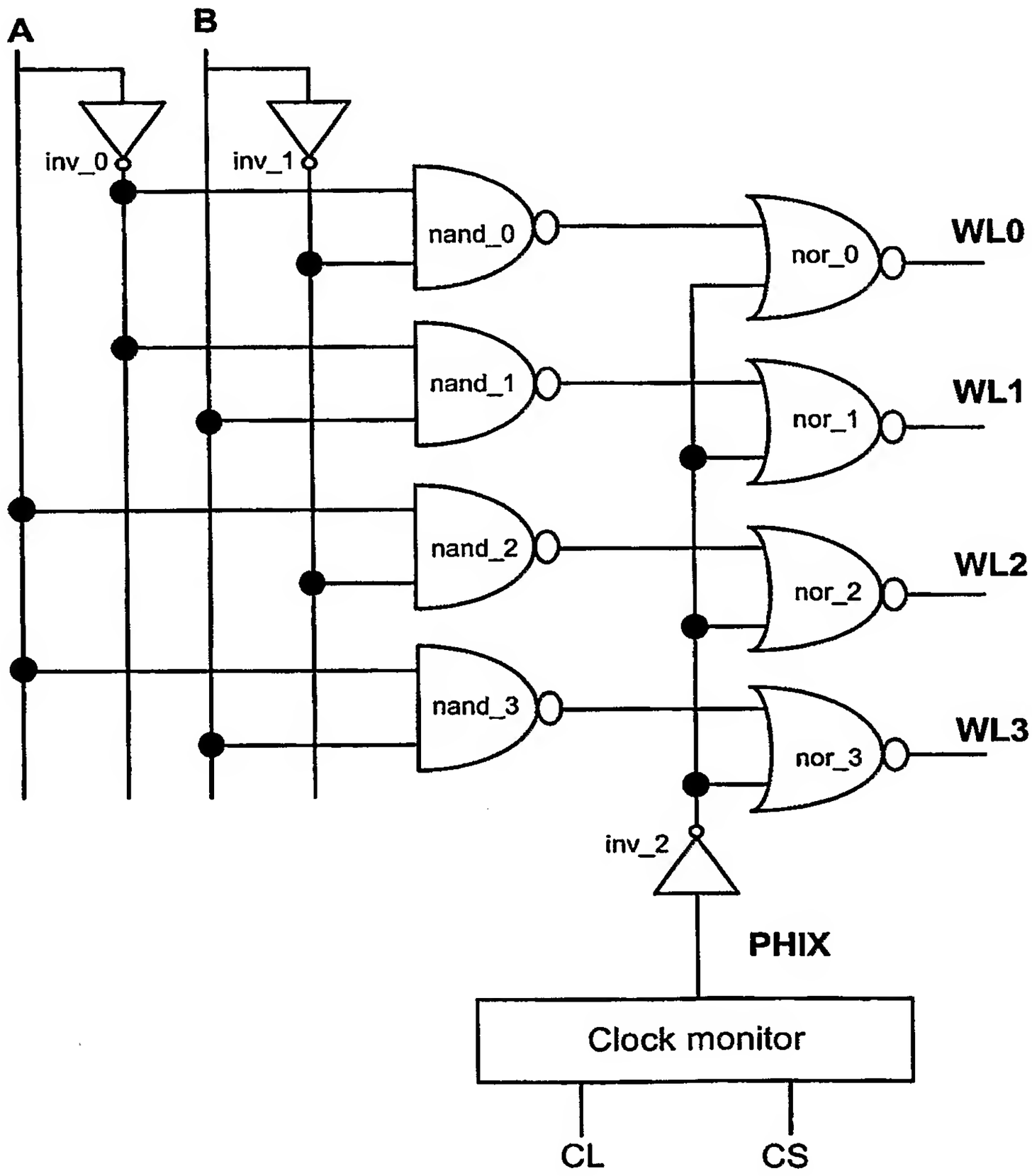

Figure 1: 2 to 4 address decoder with a clock monitor that generates the internal clock PHIX.

4. Advantages

This solution will highly increase the fault coverage of delay faults caused by either the resistive opens or bridges. By stressing the internal memory block with the external clock in test mode, the detection capability of the defects will be increased. This new DFT technique will enhance the controllability of the internal memory blocks, and therefore will enhance the fault coverage of the delay faults. As a consequence, this will lead to a better quality product, a low reliability risks and reduced customer returns (PPM).

5. Background materials

The following background references are herein incorporated by reference in their entirety.

[1] EP0531695 A2 Motorola Inc. "Self-timed random access memories"
[2] PHNL030588 EPP Koninklijke Philips Electronics N.V. "At-speed testing for resistive open defects"
[3] M. Azimane and A. Majhi, "At speed testing for resistive open defects in address decoder of semiconductor memories", TN2003/00120, Feb 2003.
[4] M. Azimane, " New test methods to detect address decoder delay faults in ROM", TN7176, Sept 2001.

Appendix A

DFT Technique for Stressing the Self-timed Semiconductor Memories to detect delay faults

Mohamed Azimane and Ananta Majhi
First draft: 22 September 2003
Last Update: 3 March 2004

Abstract

The invention introduces an efficient solution to increase the controllability to catch dynamic defects which cause delay faults and which may escape the test even when the correct test patterns are applied. The correct test patterns may result to low fault coverage when the correct stress conditions are not satisfied. The fault coverage is increased when the correct test patterns are combined with the correct stress conditions. It has been shown that a duty cycle other than 50% at the internal clock of the address decoder helps to detect the resistive open defects that lead to slow-to-rise and the slow-to-fall delays. However, nowadays the semiconductor memories are self-timed, and the corresponding actions for initiating and controlling the read and write operations are independent of the external clock. The read and write cycles in the self-timed memories are both triggered by either the positive or the negative edge of the clock. Thus, any deviation of the clock duty cycle from 50% does not disturb the function of the memory. This invention introduces a simple DFT technique to stress even more the sensitising operation by controlling internally the beginning and the end of read/write operations.

6. Problem statement

Self-timed memories are well known in the art and are used in high-speed SOCs [1]. The read and write cycles in the self-timed memories are triggered by either the rising or falling edge of the clock, the memory cycle continues until the completion independent of the falling or rising clock edge, respectively. It has been already shown in an earlier patent [2] that a duty cycle different than 50% has different effect on the delay fault coverage. A smaller duty cycle than 50% helps to detect the resistive open and bridge defects that cause slow-to-rise behaviour in the memory address decoder. A higher duty cycle than 50% helps to detect the resistive open and bridge defects that cause the slow-to-fall behaviour in the memory address decoder. Moreover, it is already known that at-speed testing stresses the delay faults when the correct test patterns are implemented [2]. However, the synthesis of the BIST logic for high frequency is not always feasible and may lead to an extra area overhead. Therefore, finding a better solution than at-speed testing helps in increasing the fault coverage of the semiconductor memories.

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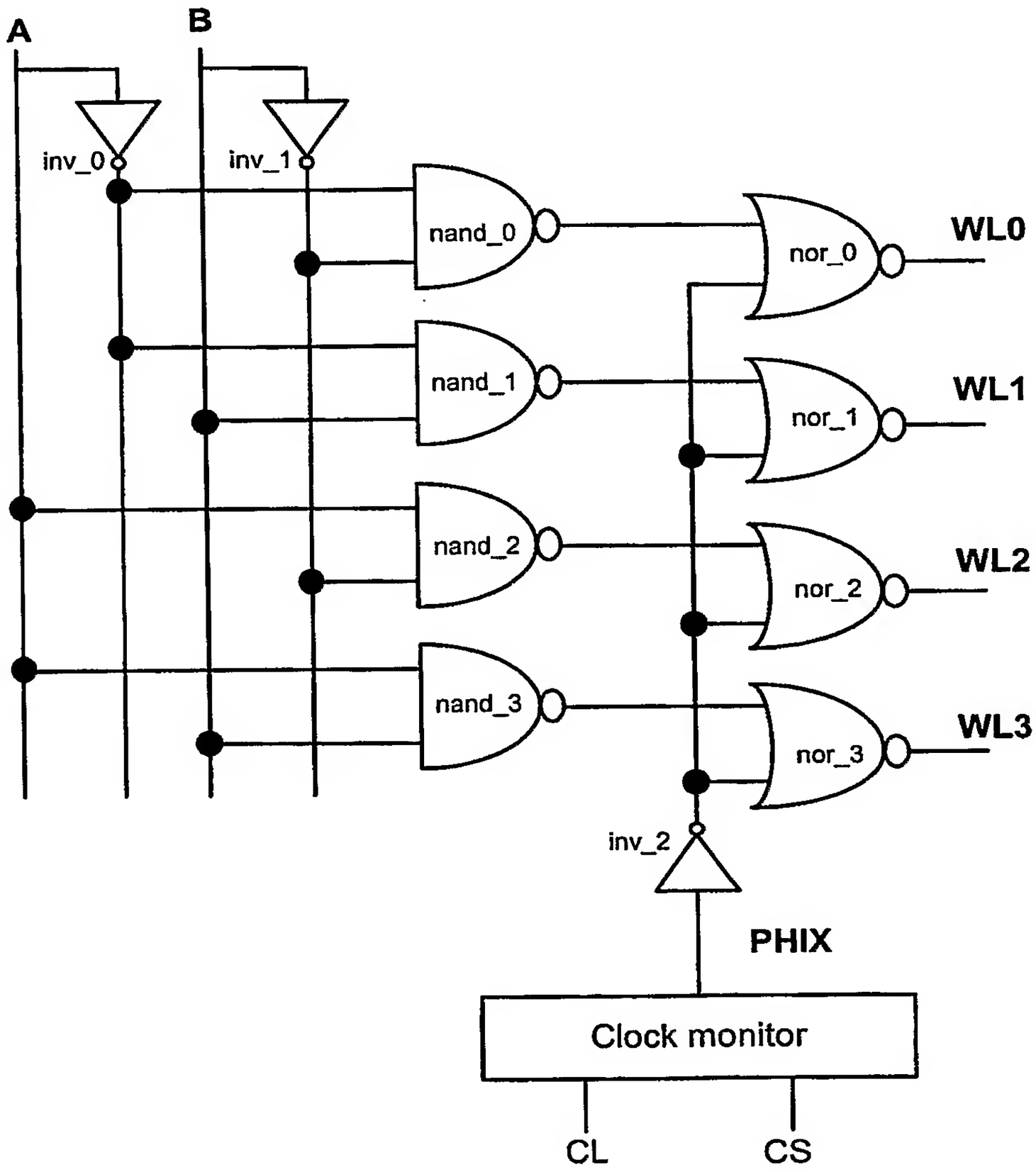
8. Proposed solution

We propose a new and efficient solution to increase the controllability of the internal block of the memory in such a way, that the duty cycle becomes a parameter which impacts the fault coverage of the delay faults. With this solution we will be able to control internally the beginning and the end of determined internal operations in the memory by introducing a simple DFT technique. Therefore, modifying the duty cycle of the clock can easily control the internal memory blocks that have a big impact on the memory fault coverage. For instance, the row address decoder is a block that can be controlled to cover small delay faults at the word lines due to weak resistive open defects. Figure 1 shows a 2 to 4 address decoder controlled by an internal clock PHIX. The control logic (i.e., the clock monitor) is initiated based on the rising or the falling edge of the external clock CL and it generates an internal clock PHIX. This controls the word line activation and deactivation depending on the rising or the falling edge of the internal clock. Hence, the deactivation of the word lines becomes independent of the external clock CL. As we have shown in patent [2], the impact of the duty cycle on the detection of the slow-to-rise and the slow-to-fall depends extensively on the waveform of the internal clock. The slow-to-rise and the slow-to-fall delay faults can only be detected by controlling the duty cycle of the internal clock and not the external clock. The internal clock of the address decoder can be easily controlled by introducing a simple MUX in between the internal clock and the external clock. In this way, the external clock will be directly applied to the

address decoder during test mode. In normal mode, the self-timed control will be operating. Thus, the beginning and the end of the activation and deactivation of the word lines will be easily controlled from the external clock. Figure 2 shows a 2 to 4 address decoder with a MUX in between the address decoder clock input and the external clock. The complete block diagram of the memory is given in Figure 3. This shows the duty cycle controller which generates the clock for the address decoders and the internal clock (PHIX) that controls the other blocks of the memory.



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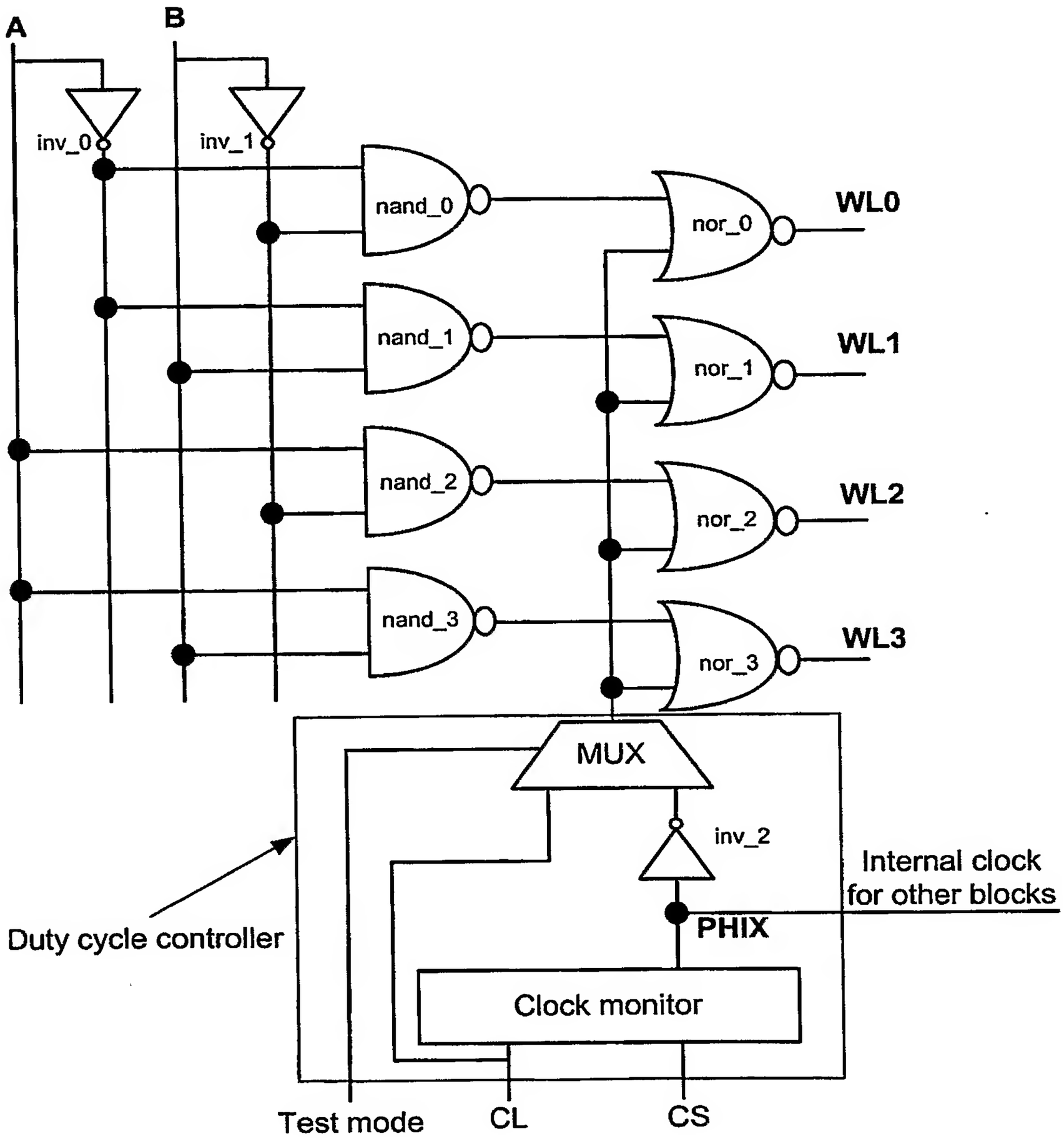


Figure 2: A simple DFT technique for controlling the self-timed memories.

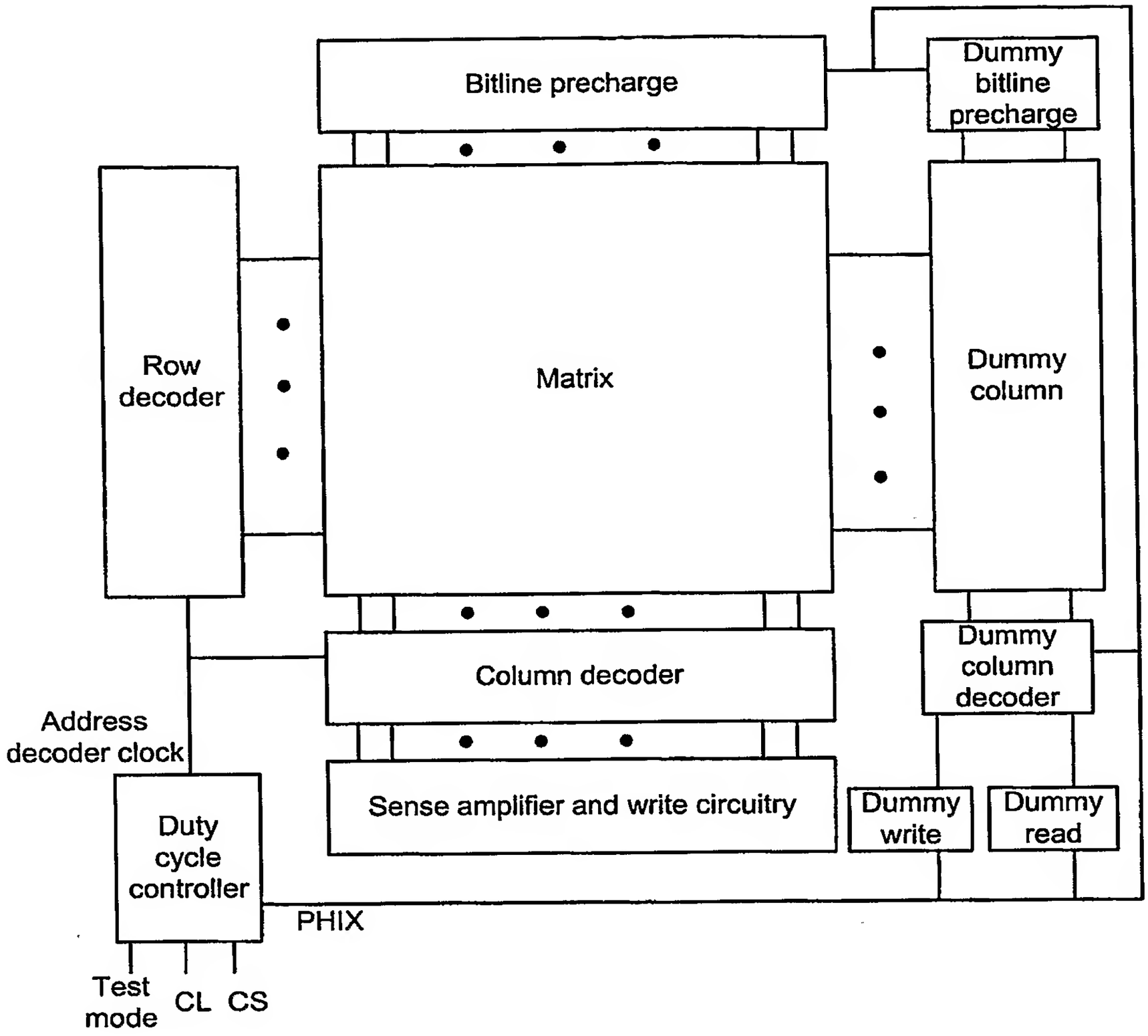
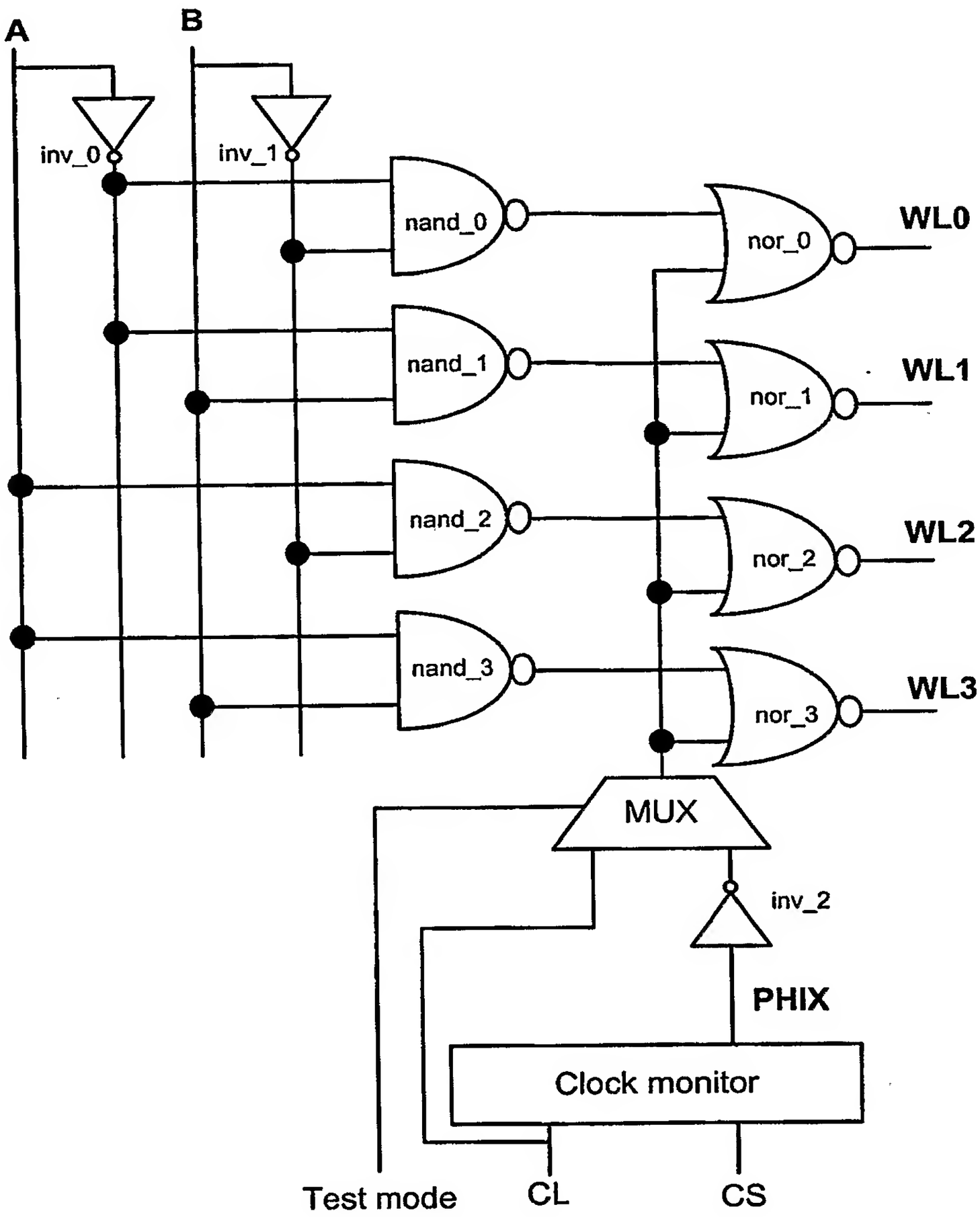


Figure 3: Global overview of the memory with the duty cycle controller.



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